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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/088,086	03/21/2002	Shouichi Fuji	221109US2PCT	7109
22850	7590	03/09/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			THAI, LUAN C	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/088,086	<b>Applicant(s)</b> FUJI ET AL.	
	<b>Examiner</b> Luan Thai	<b>Art Unit</b> 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 22 February 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 16-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 16-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 3/21/02 and 7/22/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

This Office action is responsive to the RCE filed February 22, 2005.

Claims 1-10 and 16-22 are pending in this application.

Claims 11-15 have been cancelled.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

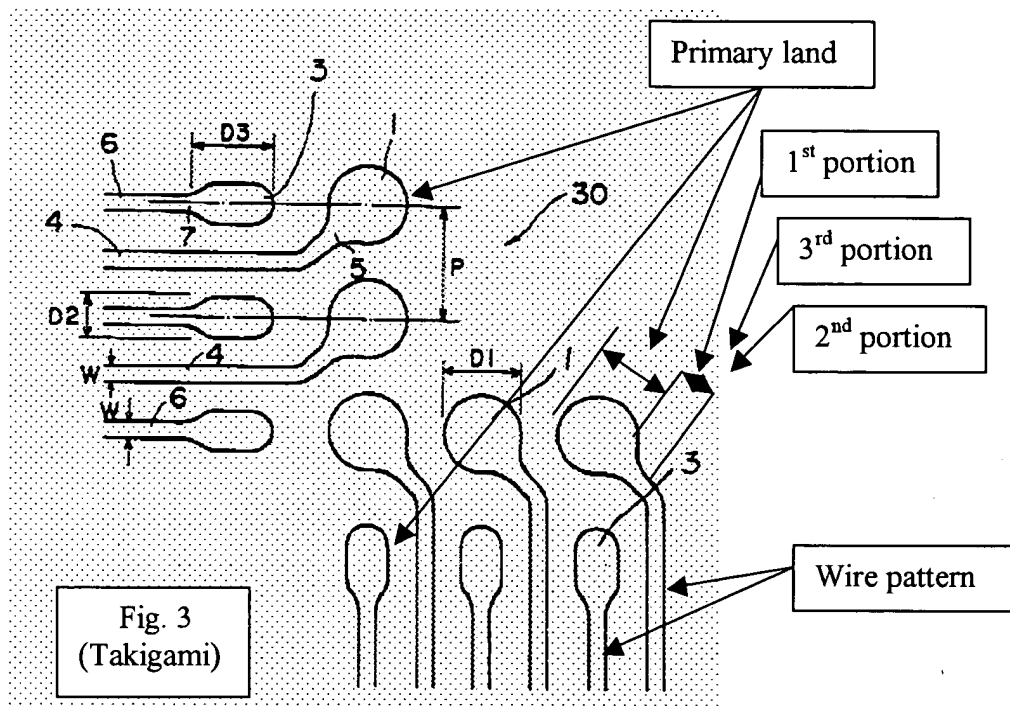
2. Claims 1-2, 4, 6-7, 10 and 16-22, insofar as being definite, are rejected under 35 U.S.C. 103(a) as being unpatentable over Howell (5,815,374 of record) in combination with Takigami (6,218,630 of record).

Regarding claims 1-2, 6-7, 10 and 16, Howell discloses (see specifically figures 6-13) an electronic component comprising: a semiconductor device (66) comprising first lands (68) electrically connected to second lands (52) of a printed wiring board (50) through solder balls (70), wherein second lands (52) comprises a primary land (52) having an circular shape and connected to a wire pattern (62) of the printed wiring board (50) and the wire pattern (62) that includes a via land having a through hole (60) in the center portion (see also figures 6-7-8), wherein the second land connects to the wire where a tensile stress is configured to be applied between the second land and the wire. Howell does not explicitly disclose *an auxiliary land (of the second land) comprising a*

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*first portion disposed adjacent the primary land and a second portion connecting to the wire, the first portion having a greater cross sectional area than the second portion, and the via land of the wire including an arcuate portion.*

Takigami while related to a similar grid array electronic component design teaches (see specifically figures 3 and 8 attached) the land-wire structures formed on the



printed circuit board (see figure 3) for electrically connecting to a semiconductor chip (see figure 8), the land-wire structures comprising: a primary lands (1/3) and an auxiliary lands (5/7) connecting to wires (4/6) where a predetermined tensile stress is configured to be applied between the lands and the wires. Takigami further discloses the primary lands (1/3) comprising a tear drop shape, and the auxiliary lands (5/7) comprising a first portion disposed adjacent the primary land and a second portion connecting to the wires including arcuate portions, the first portion having a greater cross sectional area than the

second portion, and a third portion disposed between the first and second portions, the third portion having a cross sectional area less than the first portion and greater than the second portion.

Takigami gives motivation in Col. 4, lines 63-67, and Col. 5, lines 1-4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that applying the auxiliary land structure of Takigami to Howell's invention would have been beneficial because the auxiliary land formed between the primary land and the one end of the wire and between another end of the wire and the via land of the via hole would help preventing the cut between the land and the wire by a heat shock or a heat cycle in soldering during an assembly of the semiconductor device to the printed circuit board.

Regarding claim 4, since the auxiliary land is electrically connected to the primary land in the proposed structure of Howell and Takigami, this auxiliary land is also electrically connected to the first land of the integrated circuit of the semiconductor device (via solder ball).

Regarding claims 17-19 and 21-22, Howell discloses (see specifically figures 6-13) an electronic component comprising: a semiconductor device (66) comprising at least one semiconductor land (68a/68d); a printed wiring board (50) comprising at least one board land (52a/52d) electrically connected to the at least one semiconductor land (68a/68d) via solder balls (70), the at least one board land including a primary portion (52a) having a circular shape to electrically connect to a wire pattern (62a) of a printed wiring board (50) and the wire pattern (62a) connected to the via land having a through

hole (60) formed at the center portion thereof (see figures 6-7 and 11). Howell, does not explicitly disclose *an auxiliary land comprising a first portion disposed adjacent the primary land and a second portion connecting to the wire, the first portion having a greater cross sectional area than the second portion, and the via land of the wire including an arcuate portion.*

Takigami while related to a similar grid array electronic component design teaches (see specifically figures 3 and 8 attached) the board land structure formed on the printed circuit board (see figure 3) for electrically connecting to a semiconductor chip (see figure 8), the board land comprising: a primary portion (1/3) having a circular shape and an auxiliary portion (5/7) having an about triangular shape or a tear drop shape electrically connected to wires (4/6). Takigami further discloses the auxiliary portion (5/7) comprising a first portion electrically connected to the primary portion (1/3) and a second portion configured to contact the wire (62a), the first portion having a greater cross sectional area than the second portion, and a third portion disposed between the first and second portions, the third portion having a cross sectional area less than the first portion and greater than the second portion. Takigami gives motivation in Col. 4, lines 63-67, and Col. 5, lines 1-4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that applying the auxiliary land structure of Takigami to Howell's invention would have been beneficial because the auxiliary land formed between the primary land and the one end of the wire and between another end of the wire and the via land of the via hole would help preventing the cut between the land

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and the wire by a heat shock or a heat cycle in soldering during an assembly of the semiconductor device to the printed circuit board.

Regarding claim 20, the proposed structure of Howell and Takigami discloses all elements of the claimed invention, as is noted in claim 17-19 and 21-22 above. The difference between the claimed invention and the proposed structure of Howell and Takigami is in the shape of the auxiliary portion of the board land. Claim 20 claims *a tapered shape* whereas the proposed structure of Howell and Takigami discloses *a tear drop shape* (see Takigami's figure 3). Although the proposed structure of Howell and Takigami does not teach the claimed shape of the auxiliary portion, the shape differences are not patentable unless unobvious or unexpected results are obtained from these changes. Additionally, the Applicant has presented no discussion in the specification which convinces the Examiner that the particular shape of *the auxiliary portion* is anything more than one of numerous shapes a person of ordinary skill in the art would find obvious for the purpose of smoothly connecting between the primary portion and the wire. It appears that these changes (*a tapered shape* and *a tear drop shape*) produce no functional differences and therefore would have been obvious.

3. Claims 1-10 and 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherman (5,784,262 of record) in combination with Takigami (6,218,630 of record).

Regarding claims 1-2, 6-10 and 16, Sherman discloses (see specifically figures 1-7) an electronic component comprising a semiconductor device (12) having first lands (14) electrically connected to second lands (18) of a printed wiring board (20), wherein

second lands (18) comprises a primary land (18A) having a circular shape and connected to a wire pattern (27) of the printed wiring board (20) and the wire pattern (27) connected to a via land (26A) having a through hole (22A) formed at the center portion thereof (see figures 1 and 2A-2B), wherein the second land connects to the wire where a tensile stress is configured to be applied between the second land and the wire. Sherman further discloses the via land (26A) electrically connected with the first lands at a corner of the semiconductor device (12) (see Fig. 3) and disposed so as to extend in a direction in which a warpage of the board (20) is generated in a reflow soldering step (e.g., downwardly by its own weight) (see Figs. 5 and 7). Sherman, however, does not explicitly disclose the second land comprising *an auxiliary land having a first portion disposed adjacent the primary land and a second portion connecting to the wire, wherein the first portion has a greater cross sectional area than the second portion, and the via land of the wire including an arcuate portion.*

Takigami while related to a similar grid array electronic component design teaches (see specifically figures 3 and 8 attached) the land-wire structures formed on the printed circuit board (see figure 3) for electrically connecting to a semiconductor chip (see figure 8), the land-wire structures comprising: a primary lands (1/3) and an auxiliary lands (5/7) connecting to wires (4/6) where a predetermined tensile stress is configured to be applied between the lands and the wires. Takigami further discloses the primary lands (1/3) comprising a tear drop shape, and the auxiliary lands (5/7) having an arcuate shape and comprising a first portion disposed adjacent the primary land and a second portion connecting to the wires, the first portion having a greater cross sectional area than the



second portion, and a third portion disposed between the first and second portions, the third portion having a cross sectional area less than the first portion and greater than the second portion. Takigami gives motivation in Col. 4, lines 63-67, and Col. 5, lines 1-4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that applying the auxiliary land structure of Takigami to Sherman's invention would have been beneficial because the auxiliary land formed between the primary land and the one end of the wire and between another end of the wire and the via land of the via hole would help preventing the cut between the land and the wire by a heat shock or a heat cycle in soldering during an assembly of the semiconductor device to the printed circuit board.

Regarding claims 3-4, the primary land (18), which is electrically connected to the first land (14) at the corner of the semiconductor chip (12), as shown in Sherman's figures 1 and 3, is assumed to be modified to have a structure of the auxiliary land (5) electrically connected to primary land (1), as shown in Takigami's figure 3, as described in the proposed structure of Sherman and Takigami above; thus, the auxiliary land is also electrically connected to the first land of the semiconductor chip.

Regarding claim 5, the Examiner assumes that the structure of (primary land)-(auxiliary land)-(wiring pattern) in the proposed component of Sherman and Takigami comprises the auxiliary land (5) electrically connected to primary land (1) and the wire (4) as shown in Takigami's figure 3, and the primary land (18) configured to be disposed so as to extend in a direction in which a warpage of the board (20) is generated as shown in Sherman's figures 1-3; thus, the auxiliary land, in the proposed structure of Sherman

and Takigami, is also assumed to be configured to be disposed so as to extend in a direction in which a warpage of the board is generated.

Regarding claims 17-19 and 21-22, Sherman discloses (see specifically figures 1-7) an electronic component comprising: a semiconductor device (12) comprising at least one semiconductor land (14A/14B); a printed wiring board (20) comprising at least one board land (18A/18B) electrically connected to the at least one semiconductor land (14A/14B) via solder bump (16A/16B), the at least one board land (18A/18B) including a primary portion (18A) having a circular shape and electrically connected to a wire pattern (27A), wherein the wire pattern (27A) is connected to a via land (26A), which has a through hole (22A) formed at the center portion thereof (see figures 1 and 2A-2B).

Sherman, does not explicitly disclose *an auxiliary land comprising a first portion disposed adjacent the primary land and a second portion connecting to the wire, the first portion having a greater cross sectional area than the second portion, and the via land of the wire including an arcuate portion.*

Takigami while related to a similar grid array electronic component design teaches (see specifically figures 3 and 8 attached) the board land structure formed on the printed circuit board (see figure 3) for electrically connecting to a semiconductor chip (see figure 8), the board land comprising: a primary portion (1/3) having a circular shape and an auxiliary portion (5/7) having an arcuate shape and comprising an about triangular shape or a tear drop shape electrically connected to wires (4/6). Takigami further discloses the auxiliary portion (5/7) comprising a first portion electrically connected to the primary portion (1/3) and a second portion configured to contact the wire (62a), the

first portion having a greater cross sectional area than the second portion, and a third portion disposed between the first and second portions, the third portion having a cross sectional area less than the first portion and greater than the second portion. Takigami gives motivation in Col. 4, lines 63-67, and Col. 5, lines 1-4. It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that applying the auxiliary land structure of Takigami to Sherman's invention would have been beneficial because the auxiliary land formed between the primary land and the one end of the wire and between another end of the wire and the via land of the via hole would help preventing the cut between the land and the wire by a heat shock or a heat cycle in soldering during an assembly of the semiconductor device to the printed circuit board.

Regarding claim 20, the proposed structure of Sherman and Takigami discloses the claimed invention, as is noted in claim 17-19 and 21-22 above. The difference between the claimed invention and the proposed structure of Sherman and Takigami is in the shape of the auxiliary portion of the board land. Claim 20 claims *a tapered shape* whereas the proposed structure of Howell and Takigami discloses *a tear drop shape* (see Takigami's figure 3). Although the proposed structure of Sherman and Takigami does not teach the claimed shape of the auxiliary portion, the shape differences are not patentable unless unobvious or unexpected results are obtained from these changes. Additionally, the Applicant has presented no discussion in the specification which convinces the Examiner that the particular shape of *the auxiliary portion* is anything more than one of numerous shapes a person of ordinary skill in the art would find

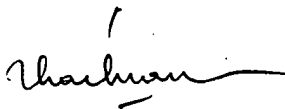
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obvious for the purpose of smoothly connecting between the primary portion and the wire. It appears that these changes (*a tapered shape* and *a tear drop shape*) produce no functional differences and therefore would have been obvious.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**Luan Thai**

Primary Examiner

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March 5, 2005